Attorney Docket No. 16869N-031100
Client Ref. No. NT0419US

PATENT APPLICATION

Optical Modules and Methods of Making the Optical Modules

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TITLE OF THE INVENTION

OPTICAL MODULES AND METHODS OF MAKING THE OPTICAL MODULES

BACKGROUND OF THE INVENTION

The present invention relates to optical modules and methods of making the optical modules, or electronic devices using the optical modules and optical communication systems using the optical modules.

Fig. 13 is a configuration diagram showing a conventional optical module with a jitter transfer bandwidth being adjusted and Fig. 14 is a flow chart showing an example of procedure from assembly to shipment of the conventional optical module.

As shown in Fig. 13, a optical receiver 65 has a PD or APD 66 for conversion from a light signal into an electric signal, a transimpedance amplifier 67 for current/voltage conversion, a voltage amplifier 68, and a CDR IC 27. The CDR IC 27 has a PLL 13 which comprises a phase detector 4, a filter circuit 7 and a VCO 12, a decision circuit 14, a data output buffer 15, and a clock output buffer 16.

In adjusting a jitter bandwidth of the optical module (CDR IC 27), an output signal from a pulse pattern generator 76 is converted to a light signal by means of a standard optical transmitter 75, which light signal is inputted to the optical receiver 65 through an optical fiber 64, and a clock output 65b from the optical receiver 65 is measured by means of a jitter

analyzer 77.

As shown in Fig. 14, a conventional optical module manufacturing process is divided into an optical module assembling step (including the installation of CDR IC 27), an adjusting step (an optical module jitter transfer bandwidth adjusting step), and a test step.

Thus, after assembly of the optical module, the sensitivity of APD is adjusted and the jitter transfer bandwidth is measured. If the jitter transfer bandwidth satisfies a prescribed standard, the receiving module is tested for operation and is shipped if it passes the test. On the other hand, if the jitter transfer bandwidth does not satisfy the standard, a resistor R11 is replaced and the jitter transfer bandwidth is measured again. This is repeated until satisfying the standard for the jitter transfer bandwidth.

For example, on page 3 of a catalog (MP1777A-J-A-1-(4.00), November 22, 2000) of Anritsu MP1777A there is described adjusting the jitter transfer bandwidth with use of a pulse pattern generator and a jitter analyzer. In the conventional jitter transfer bandwidth adjustment, CDR IC is operated at an actual speed.

SUMMARY OF THE INVENTION

However, in the conventional optical module manufacturing process it is necessary to use the expensive pulse pattern generator 76 and jitter analyzer 77 and the assembly of the module

is followed by manual replacement of a resistor, requiring 10 minutes or so.

More particularly, the higher the operating frequency, the more expensive the pulse pattern generator and the jitter analyzer, and it takes several minutes for the measurement, thus resulting in an increase of the adjustment cost.

Besides, since the operation is performed at an actual speed, it is necessary that a signal be inputted to the IC at the same speed as in actual operation. Consequently, in a CDR IC of a high speed such as 2.5 Gbps or 10 Gbps, such a high-speed signal as 2.5 Gbps or 10 Gbps is not allowed to pass in a normal probe, so it is difficult to adjust the jitter transfer bandwidth, for example, by trimming a resistor in IC at the time of DC test for the IC, and it has so far been required to make the adjustment by using external resistor and capacitor after mounting the circuit board of module.

It is an object of the present invention to decrease the adjustment cost in the manufacture of an optical module and thereby provide a less expensive optical module.

It is another object of the present invention to provide a jitter transfer bandwidth adjusting method for an optical module less expensively.

The following is a brief description of typical inventions out of those disclosed herein for achieving the above-mentioned object.

In one aspect of the present invention there is provided an optical module including a photodiode or an avalanche photodiode for converting a light signal into an electric signal, a transimpedance amplifier for current/voltage conversion, a voltage amplifier, and a clock and data recovery IC, the clock and data recovery IC being subjected to adjustment of a jitter transfer bandwidth before being mounted on the optical module.

In another aspect of the present invention there is provided the above optical module wherein the clock and data recovery IC includes a phase locked loop, the phase locked loop comprising a voltage-controlled oscillator, a phase shifter for changing the phase of an output signal provided from the voltage-controlled oscillator, a selector for selecting either data provided from a data input pad or an output from the voltage-controlled oscillator, a phase detector, and a filter circuit which inputs an output signal from the phase detector and which provides an output signal to the voltage-controlled oscillator.

In a further aspect of the present invention there is provided an optical module including a photodiode or an avalanche photodiode for converting a light signal into an electric signal, a transimpedance amplifier for current/voltage conversion, a voltage amplifier, and a clock and data recovery IC, the clock and data recovery IC has a phase locked loop, the phase locked loop comprising a voltage-controlled oscillator, a +45 phase shifter for causing the phase of one branched output signal from

the voltage-controlled oscillator to lead 45°, -45 phase shifter for causing the phase of the other branched output signal from the voltage-controlled oscillator to lag 45°, a selector for selecting either data provided from a data input pad or an output from the -45 phase shifter, a phase detector which compares the phase of the output selected by the selector with the phase of an output from the +45° phase shifter, and a filter circuit which receives an output from the phase detector and which provides an output signal to the voltage-controlled oscillator.

In a still further aspect of the present invention there is provided an optical module manufacturing method comprising the steps of adjusting a jitter transfer bandwidth of a clock and data recovery IC, mounting the thus-adjusted clock and data recovery IC onto an optical module, and mounting a photodiode or an avalanche photodiode which is for conversion from a light signal into an electric signal, a transimpedance amplifier which is for current/voltage conversion, and a voltage amplifier. It goes without saying that the jitter transfer bandwidth may be finely adjusted after mounting of the adjusted clock and data recovery IC.

In a still further aspect of the present invention there is provided an optical module manufacturing method wherein, in the step of adjusting the jitter transfer bandwidth of the clock and data recovery IC, the clock and data recovery IC includes a data input pad, a data output pad, a clock output pad, a phase

detector, a voltage-controlled oscillator, and a phase shifter for changing the phase of an output waveform from the voltage-controlled oscillator, and at least two output waveforms outputted from the voltage-controlled oscillator and about 90° out of phase with each other are inputted to the phase detector.

In a still further aspect of the present invention there is provided an optical communication system including a multiplexer for time-multiplexing a signal, a optical transmitter, an optical fiber for the transmission of a light signal outputted from the optical transmitter, a optical receiver which receives a light signal from the optical fiber and converts it into an electric signal and which reproduces a clock, and a demultiplexer which separates the electric signal, the optical receiver being any of the foregoing optical modules.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram illustrating a CDR IC according to the first embodiment of the present invention;

Fig. 2 illustrates a characteristic of a filter circuit in the CDR IC;

Fig. 3 illustrates waveforms of various portions in normal operation of the CDR IC;

Fig. 4 is a circuit diagram showing a circuitry in adjusting a jitter transfer bandwidth of the CDR IC;

Fig. 5 illustrates a method for measuring a VCO modulation

sensitivity in jitter adjustment for the CDR IC;

Fig. 6 illustrates waveforms of various portions in jitter adjustment for the CDR IC;

Fig. 7 is a circuit diagram illustrating a CDR IC according to another embodiment of the present invention;

Fig. 8 is a circuit diagram illustrating a CDR IC according to a further embodiment of the present invention;

Fig. 9 is a circuit diagram illustrating a CDR IC according to a still further embodiment of the present invention;

Fig. 10 illustrates waveforms of various portions in jitter adjustment for the CDR IC shown in Fig. 9;

Fig. 11 illustrates a configuration of an optical communication system;

Fig. 12 illustrates a jitter transfer characteristic of an optical communication module and CDR IC;

Fig. 13 illustrates a configuration in adjusting a jitter transfer bandwidth of a conventional optical module;

Fig. 14 is a flow chart showing an example of procedure from assembly to shipment of the conventional optical module; and

Fig. 15 illustrates a still further embodiment using a CDR IC.

DETAILED DESCRIPTION OF THE EMBODIMENTS

An optical module according to the present invention and

a method of making the optical module, especially a jitter transfer bandwidth adjusting method, will be described below with reference to drawings.

First, an example of an optical communication system using the optical module according to the present invention will be described with reference to Fig. 11. In the same figure, an optical communication system comprises a multiplexer 60 for time-multiplexing a signal which has been subjected to a processing such as switching, a optical transmitter 61, an optical fiber for the transmission of a light signal outputted from the optical transmitter 61, a optical receiver 65 which receives a signal from the optical fiber 64 and converts it into an electric signal and which reproduces a clock, and a demultiplexer 70 which separates a signal so as to facilitate a digital processing.

The optical transmitter 61, which receives a data signal 61a and a clock signal 61b from the multiplexer 60, has a laser diode 63 and a driver IC 62 for driving the laser diode 63.

The optical receiver 65 has a photodiode ("PD" hereinafter) or an avalanche photodiode ("APD" hereinafter) for conversion from a light signal into an electric signal, a transimpedance amplifier 67 for current/voltage conversion, a voltage amplifier 68, and a CDR IC 69.

Usually, only the data signal is transmitted to the optical fiber.

Both data signal and clock signal are needed for processing

in a digital system, so in the optical receiver a clock signal is extracted from a data signal in CDR IC and waveform is re-shaped using the clock.

In a signal 64a which is transmitted through the optical fiber there occurs a jitter, tj, due to a waveform distortion which the driver IC has, a waveform distortion induced at the time of electro-optical conversion in the laser diode 63, or a waveform distortion based on a dispersion characteristic of the optical fiber 64. The jitter is added when such an optical communication system as shown in Fig. 11 is cascade-connected, making the proper signal transmission impossible. In the CDR IC, therefore, it is necessary to suppress the jitter at a certain frequency, ft, or higher as in Fig. 12. The frequency, ft, and the jitter suppressing quantity are defined by a standard, so the optical receiver must observe the standard.

The CDR IC used in the optical module according to the present invention will be described below with reference to Figs. 1, 2 and 3. Fig. 1 is a circuit diagram showing a CDR IC of the first embodiment used the optical module according to the present invention.

In Fig. 1, the CDR IC, indicated at 27, is made up of a PLL (phase locked loop) 13, a decision circuit 14, a data output buffer 15, and a clock output buffer 16, the PLL 13 comprising a +45° phase shifter 1, a -45° phase shifter 2, a data input pad 20, a selector 3 for selecting either data provided from

a data input pad 20 or an output from the -45 phase shifter 2, a phase detector 4, a filter circuit 7, and a VCO (voltage-controlled oscillator) 12, the phase detector 4 comprising a sample & hold type phase detecting portion 5 for comparing the phase of an output signal provided from the selector 3 with the phase of an output signal provided from the +45° phase shifter 1 and a variable gain portion 6 capable of changing the amplification factor by trimming the resistance value in the circuit capable of providing a high impedance output in accordance with a signal from a test pad 21, the filter circuit 7 comprising an amplifier circuit portion 8 capable of providing a high impedance output in accordance with a signal from a test pad 22, a resistor 9 located within the IC, and external capacitor 10 and resistor 11 both connected to the resistor 9 through a pad 24, the filter circuit 7 having such a lag-lead characteristic as shown in Fig. 2.

In this embodiment, the CDR IC 27 has two operational states capable of being switched from one to the other by the test pads 21 and 22. One is a state ("normal operation" hereinafter) in which the IC is mounted on the optical module and a clock signal is reproduced from an input data signal, and the other is a state ("jitter transfer bandwidth adjustment" hereinafter) in which in a DC test of IC before mounting on the optical module a jitter transfer bandwidth is measured for adjustment.

In normal operation, the selector 3 is set so that a signal

obtained by causing the output of VCO 12 to lead 45° and a signal provided from the data input pad 20 are fed to the phase detector 4, while in jitter transfer bandwidth adjustment the selector 3 is set so that a signal obtained by causing the output of VCO 12 to lead 45° and a signal obtained by causing the output of VCO 12 to lag 45° are fed to the phase detector 4.

Now, with reference to Fig. 3, a description will be given below about the normal operation of the CDR IC 27.

Fig. 3 shows a relation among the waveform of an input 4a to the phase detector 4 obtained by causing the output of VCO 12 to lead 45°, an input waveform 4b from the data pad 20 to the phase detector 4, and an output waveform 4c from the phase detecting portion 5 in the phase detector 5. Although the waveform 4b from the data input pad 20 is originally a random pattern, it is represented in terms of alternate Hi and Low waveforms for ease of explanation.

At a leading edge of the waveform 4b from the data input pad 20 the phase detecting portion 5 in the phase detector 4 samples and holds the waveform 4a obtained by causing the output of VCO 12 to lead 45°. Therefore, at time t1, the output 4c from the phase detecting portion 5 in the phase detector 4 has an amplitude of the output waveform from VCO 12. This voltage is inputted to VCO 12 via the variable gain portion 6 in the phase detector 4 and the filter 7, making low the frequency generated from VCO 12 and shifting the phase of the 45°-leading

waveform 4a from the output of VCO 12 relative to the waveform 4b provided from the data input pad 20. In this way PLL 13 operates so that the waveform 4b from the data input pad 20 and the 45°-leading waveform 4a from the output of VCO 12 are put in phase with each other.

Next, with reference to Figs. 4, 5 and 6, the following description is provided about the operation of CDR IC 27 in jitter transfer bandwidth adjustment.

Fig. 4 is a circuit diagram of the CDR IC 27 in jitter transfer bandwidth adjustment. In the same figure, a switch 51 capable of selecting a variable voltage source 52 and a voltmeter 50 is connected to a pad 23 which is provided at an output of the phase detector 4 in the CDR IC 27, while to a pad 24 provided in the filter circuit 27 is connected a switch 53 which can select, instead of the capacitor 10 and resistor 11, a variable voltage source 54 and a resistor 55 having the same resistance value as the resistor 11.

The jitter transfer bandwidth, ωjt, is represented by the following Expression (1):

$$\omega jt = Kd \times Ad \times Kh \times Ko \qquad \ldots(1)$$

where Kd stands for a detection sensitivity of the phase detecting portion 5 in the phase detector 4, Ad stands for an amplification factor of the variable gain portion 6 in the phase detector 4, Kh stands for an amplification factor at frequency f2 or higher of the filter circuit 7 having such a lag-lead characteristic

as shown in Fig. 2, and Ko stands for a modulation frequency of VCO 12.

For adjusting the jitter transfer bandwidth, first Kh x Ko is measured and then the amplification factor of the variable gain portion 6 in the phase detector 4 is adjusted by trimming the resistance value so as to give a desired jitter transfer bandwidth.

Kh x Ko is measured in the following manner. In Fig. 4, the test pad 22 is set so as to give a high impedance output from the variable gain portion 6 in the phase detector 4, the switch 51 is set for connection with the variable voltage source 52, and the switch 53 is set for connection with the resistor 55. Then, as shown in Fig. 5, the variable voltage source is set at voltages V1 and V2 near a voltage V0 at which the frequency of a signal outputted from a clock output pad 26 becomes equal to a lock frequency f0 of the CDR IC 27, and the frequency of a signal outputted from the clock output pad 26 is measured. Given that the frequency of a signal outputted from the clock output pad 26 at voltage V1 is f1 and that of a signal outputted from the clock output pad 26 at voltage V2 is f2, Kh x Ko can be represented by the following Expression (2):

$$Kh \times Ko \fallingdotseq (f2 - f1)/(V2 - V1) \quad \ldots (2)$$

Next, in Fig. 4, the test pad 21 is set so that the selector 3 is set to have a 45°-leading signal from the output of VCO 12 and a 45°-lagging signal from the VCO output applied to the

phase detector 4 and so that the amplifier portion in the filter circuit 7 provides a high impedance output. Likewise, the test pad 22 is set so that the variable gain portion 6 in the phase detector 4 operates as an amplifier circuit, the switch 51 is set for connection with the voltmeter 50, the switch 53 is set for connection with the voltage source 54, and the voltage source 54 is set so that the frequency of a signal outputted from the clock output pad 26 becomes f0. The value of the voltmeter 50 is equal to Kd x Ad, so for adjustment into a desired jitter transfer bandwidth ωjt, the amplification factor of the variable gain portion 6 in the phase detector 4 is adjusted so as to be ωjt/(Kh x Ko), for example, by trimming the resistance value.

The reason why the value of the voltmeter 50 is equal to Kd x Ad will be stated below with reference to Fig. 6.

The signal 4a resulting from leading the output of VCO 12 by 45° and a signal resulting from lagging the output of VCO 12 by 45° are inputted to the phase detector 4. As the phase detecting portion 5 in the phase detector 4 there is used a sample & hold type. When the output signal from VCO 12 is sinusoidal, the 45°-leading signal 4a from the output of the VCO 12 and the 45°-lagging signal 4b from the VCO 12 are 90° out of phase with each other, so the output of the phase detecting portion 5 exhibits the same value of amplitude as the amplitude Vp of the output signal from VCO 12. Moreover, in the case where the output signal from VCO 12 is sinusoidal, the detection sensitivity of the phase

detecting portion 5 in the phase detector 4 in phase-locked condition of CDR IC 27 corresponds to a gradient at t5 of the output signal from VCO 12 as in Fig. 3, so the value thereof becomes equal to the amplitude Vp of the output signal from VCO 12.

This is because the output 4a of VCO 13 is represented by the following Expression (3) if it is sinusoidal:

$$4a = Vp\sin(\omega t) \qquad \ldots (3)$$

The gradient $\triangle$ of the waveform 4a is represented by differentiation of Expression (3) and is therefore:

$$\triangle = Vp\cos(\omega t) \qquad \ldots (4)$$

Since t5 in phase lock condition is equal to the point of t = 0:

$$\triangle = Vp \qquad \ldots (5)$$

Accordingly, the detection sensitivity of the phase detecting portion 5 in the phase detector 4 is equal to the amplitude Vp of the output signal in VCO 12.

Thus, the reading on the voltmeter 50 becomes equal to Kd x Ad, and by adjusting the value of Ad by trimming it becomes possible to adjust the jitter transfer bandwidth of CDR IC 27 to a desired value.

Although in Fig. 1 the filter circuit 7 is composed of the amplifier circuit portion 8, resistor 9 in the IC and external capacitor 10 and resistor 11, it is not always necessary to adopt such a configuration insofar as there is obtained such a lag-lead

characteristic as shown in Fig. 2.

In jitter transfer bandwidth adjustment it suffices for a 90°-shifted output of VCO 12 to be inputted to the phase detecting portion 5 in the phase detector 4 and therefore a +90° phase shifter 17 may be connected between VCO 12 and the phase detector 4, as shown in Fig. 7. Further, as shown in Fig. 8, a -90° phase shifter 18 may be connected between the VCO 12 and the selector 3.

In case of using both +45° phase shifter and -45° phase shifter, it is possible to let a phase difference of 90° occur constantly because phase shifts resulting from circuit characteristics of the phase shifters offset each other.

According to this embodiment, since the gain of the variable gain portion 6 in the phase detector 4 is changed by resistance trimming and it is thereby possible to adjust the jitter transfer bandwidth, it is not required to make adjustment at the time of assembling the module. Consequently, it becomes possible to reduce the cost of the optical receiver.

Besides, as shown in Fig. 4, the adjustment of the jitter transfer bandwidth can be made using the voltage sources 52, 54, the voltmeter 50 and the frequency meter 90 without using the expensive pulse pattern generator 76 and jitter analyzer 77, thus making it possible to reduce the cost of the optical receiver.

Fig. 9 is a circuit diagram illustrating a CDR IC in an

optical module according to a further embodiment of the present invention.

In the same figure, the CDR IC of this embodiment, indicated at 27, comprises a PLL (phase locked loop) 13, a decision circuit 14, a data buffer 15, and a clock buffer 16, the PLL 13 comprising a +45° phase shifter 1, a -45° phase shifter 2, a frequency divider 19 connected to an output of the -45° phase shifter 2, a selector 3 for selecting either an output from a data input pad 20 or an output from the frequency divider 19, a phase detector 4, a filter circuit 7, and a VCO (voltage-controlled oscillator) 12, the phase detector 4 comprising a sample & hold type phase detecting portion 5 for comparing the phase of an output from the selector 3 with that of an output from the +45° phase shifter 1 and a variable gain portion 6 capable of changing the amplification factor by trimming the resistance value in the circuit and capable of providing a high impedance output in accordance with a signal from a test pad 21, the filter circuit comprising an amplifier circuit portion 8 capable of providing a high impedance output in accordance with a signal from a test pad 22, a resistor 9 in the IC, and external capacitor 10 and resistor 11 connected to the resistor 9 through a pad 24, the filter circuit 7 having such a lag-lead characteristic as shown in Fig. 2.

In Fig. 9, the test pad 21 is set so that the selector 3 is set to have a 45°-leading signal from the output of VCO

12 and a 45°-lagging signal from the VCO output applied to the phase detector 4 and so that the amplifier portion 8 in the filter circuit 7 provides a high impedance output.

Likewise, the test pad 22 is set so that the variable gain portion 6 in the phase detector 4 operates as an amplifier circuit, a switch 51 is set for connection with a voltmeter 50, a switch 53 is set for connection with a voltage source 54, and the voltage source 54 is set so that the frequency of a signal outputted from a clock output pad 26 becomes f0. The resulting waveform is as shown in Fig. 10.

In Fig. 10, indicated at 4a is the waveform of an input 4a of the phase detector 4 obtained by causing the output of VCO 12 to lead 45°, indicated at 2a is the waveform of an output 2a of the phase shifter 2 obtained by causing the output of VCO 12 to lag 45°, indicated at 19a is the waveform of an output 19a of the frequency divider 19 obtained by dividing the waveform 2a to a half with the frequency divider 19, and indicated at 4c is the waveform of an output 4c of the phase detecting portion 5 in the phase detector 4.

Since sampling points t1 and t2 of the phase detecting portion 5 in the phase detector 4 become peak points of the waveform 4a, the output of the phase detecting portion 5 takes the same value as the amplitude Vp of an output signal from VCO 12 and thus it is possible to obtain a detection sensitivity of the phase detecting portion 5.

In the configuration of Fig. 1, since the signal 4b in normal operation is a data signal, the frequency thereof is a half or less of the signal 4b in jitter transfer bandwidth adjustment which signal is a clock signal. That is, the circuit in which the signal 4b is inputted in the phase detecting portion 5 of the phase detector 4 requires an operating frequency twice as high as that in normal operation, so that there occurs a wasteful portion in the circuit due to the resulting necessity of allowing a large amount of current to flow to permit a high-speed operation.

In the configuration of Fig. 9, it suffices for the phase detecting portion 5 in the phase detector 4 to sample and hold with a cycle which is half of that in the configuration of Fig. 1. Thus, it becomes easier to make a circuit design in the case where the CDR IC handles a high-speed signal. Further, in case of using the same circuit, it is possible to use a frequency up to twice as high.

Although in Fig. 9 there are used both +45° and -45° phase shifters, there may be used a +90° or -90° phase shifter as in Figs. 7 and 8.

Fig. 15 is a configuration diagram using a CDR IC according to a further embodiment of the present invention.

In the same figure, a server or router 88 is composed of a substrate with plural multiplexers 80 and transmission line drivers 81 mounted thereon, a substrate 87 with plural receiving amplifiers 82, CDR ICs 83 and demultiplexers 84 mounted thereon, and plural

transmission lines 85 for connection between both substrates.

In the case of a server, CPUs are mounted on the substrates 86 and 87, while in the case of a router, switching ICs are mounted on the substrates. The transmission lines 85 are, for example, coaxial or twisted pair cables or lines formed on a substrate. In a server or a router, a signal exceeding 1GHz is allowed to flow in the transmission lines 85 for increasing the amount of data transmitted between the substrates and for decreasing the number of cables and of signal lines on the substrates to reduce the manufacturing cost. With such a signal exceeding 1GHz, it is difficult to phase data and clock with each other and therefore only the data signal is transmitted, while clock is reproduced in the CDR IC 83.

For the CDR IC 83 a jitter standard is established as is the case with the optical receiver and for observing the standard it is necessary to adjust the jitter transfer bandwidth. Since plural CDR ICs are mounted on a substrate, several ten minutes to several hours are needed for the adjustment, but according to the present invention all that is required is a mere mounting of IC, thus making it possible to reduce the cost of the server or router.

According to the present invention, the cost for adjustment at the time of assembling the optical module is reduced, thereby permitting the provision of a less expensive optical module.